Quiz 4

(November 19th @ 5:30 pm)

PROBLEM 1 (35 PTS)

- Draw the state diagram (in ASM form) of the FSM whose VHDL description is listed below:

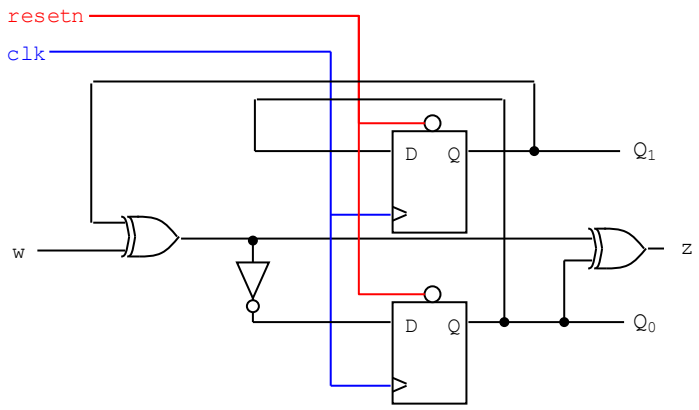
```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, rstn: in std_logic;
          r, p, q: in std_logic;
          x, w, z: out std_logic);
end circ;
```

```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (rstn, clk, r, p, q)
  begin
     if rstn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if r = '1' then y <= S2;
            else if p = '1' then y <= S3; else y <= S1; end if;
            end if;

          when S2 =>
            if p = '1' then y <= S1; else y <= S3; end if;

          when S3 =>
            if q = '1' then y <= S3; else y <= S2; end if;

        end case;
     end if;
  end process;

  Outputs: process (y, r, p, q)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if r = '0' then x <= '1'; end if;
         when S2 => if q = '0' then w <= '1'; end if;
                    if p = '0' then z <= '1'; end if;
         when S3 => if q = '0' then w <= '1'; end if;
      end case;
  end process;
end behavioral;
```

- ✓ Circle or mark the correct FSM type:
  (Mealy) (Moore)

PROBLEM 2 (35 PTS)

- Given the following FSM circuit:
  - ✓ Provide the Excitation Table and the Excitation equations (including the Boolean equation for z).



- Is this a Mealy or a Moore FSM? Why? (5 pts)

PROBLEM 3 (30 PTS)

- Sequence detector: Draw the state diagram (any representation) of an FSM with input x and output z. The detector asserts $z = 1$ when the sequence 0110 is detected. Right after the sequence is detected, the circuit looks for a new sequence.